

ECE186 SPRING 2002 SUGGESTED PROJECT DEBUGGING SEQUENCE SUGGESTED WIRING & DEBUGGING SEQUENCE:

1. Wire PLD. Static Test PLD(If necessary, see Course Instructor for jumper wires). * At this stage, the 68000 processor should NOT be plugged in. * Use jumper wires to provide logic inputs to PLD according to TRUTH TABLE. * Observe PLD outputs for the corresponding 'Chip_Select' signals
2. Wire the EPROM. Do Normal(Dynamic) Test of ROM . * CPU should be installed in its socket.
3. Burn the ROM_TEST program into ROM. This program is referred to as ASTEST on page 162 of the Lecture Notes. The same program is referred to as AS_TEST on page 22 of Danny Lyda's report. This is a short Program(Branch To Itself). Use Scope to monitor AS, DTACK, R/W, ROM_CS. * Make sure your software program has been thoroughly tested(simulated, debugged) with the 68000 emulator. * If your hardware does not seem to be working, try meticulous visual checking of your EPROM wiring. * Still not working? Remove the CPU and do STATIC TESTING of the EPROM.
4. Static Test(i.e. with CPU removed) LATCH and LED(Static Write to LEDs). Static Test(CPU NOT in socket) DIP SW(Read from Dip Switch).
5. Static Test RAM(Write to RAM). Read from RAM.
6. Do normal testing(with CPU in socket and appropriate programs having been burned into EPROM). Run Counting Program on LED. Program to Read from SW. See testing software examples from pages 162-165 of Lecture Notes and also from pages 22-28 of Danny Lyda's report.
7. Test A/D or D/A 8. Test UART