

TOPIC OF INTEREST:

- INTERFACING MICROPROCESSORS TO MEMORY:
ADDRESS DECODING TECHNIQUES.
- EIGHT-BITS AND SIXTEEN-BITS EXAMPLES

READING ASSIGNMENT:

- CLEMENTS: SECTIONS 5.1 AND 5.2
- LECTURE NOTES: PAGES 78-86

KEY WORDS:

MEMORY MAP, ADDRESS MAP, ADDRESS DECODING TABLE, BLOCK DECODING, FULL DECODING, PARTIAL DECODING, CHIP SELECT SIGNALS, OUTPUT ENABLE, WRITE ENABLE.

KEY DEFINITIONS:

- MEMORY MAP/ADDRESS MAP: LAYOUT OF SLOTS IN PROCESSOR'S ADDRESS SPACE OCCUPIED BY MEMORY & I/O COMPONENTS.
- ADDRESS DECODER: LOGIC CIRCUIT WHOSE INPUTS ARE ADDRESS & APPROPRIATE CONTROL SIGNALS FROM THE PROCESSOR, AND WHOSE OUTPUTS SELECT CORRESPONDING MEMORY OR I/O DEVICES.
- BLOCK DECODING: DIVIDING MEMORY MAP INTO EQUAL BLOCKS.
- FULL DECODING: INCLUDING ALL OF PROCESSOR'S ADDRESS LINES IN THE DECODING PROCESS.
- PARTIAL DECODING: USING ONLY SOME OF PROCESSOR'S ADDRESS LINES FOR DECODING.
- OUTPUT ENABLE INPUT: ACTIVATION CONNECTS MEMORY OR I/O'S TRI-STATED OUTPUT TO THE DATA BUS.
- CHIP SELECT SIGNAL: SIGNAL USED TO SELECT AND ACTIVATE MEMORY OR I/O WHEN MEMORY OR I/O'S ADDRESS IS PRESENTED TO THE ADDRESS DECODER'S INPUT.

ADDRESS DECODER DESIGN : REFER TO EXAMPLES IN NOTES & TEXTBOOK

- DEVELOP MEMORY OR ADDRESS MAP
- FROM MEMORY MAP GENERATE ADDRESS DECODING TABLE
- DESIGN THE LOGIC OF THE DECODER
- GENERATE INTERCONNECTION AMONG PROCESSOR, DECODER, MEMORY & I/O'S