

## EECE-315 Prelab 10

In this lab, you will be verifying the JFET bias design that you did in the homework problem.

1. Check back to the homework problem and record the values of all components used in the bias circuits, including the supply voltage.
2. Also record the PSpice values of the worst-case maximum and minimum DC drain current.

## EECE-315 Lab 10

1. Use a 2N3819 JFET to build up the bias circuit that you designed. The drain resistance should be zero. Measure  $I_{DQ}$  and  $V_{DSQ}$ . Make sure that you measure all resistance values.
2. Use a curve tracer to find the  $I_{DSS}$  and  $V_P$  (at least 2 significant figures) of your 2N3819 JFET. Print a hard copy. Add a load line to the curve tracer plot and show the Q-point corresponding to your design
3. Use the measured  $I_{DSS}$ ,  $V_P$  and resistance values to calculate the theoretical  $I_{DQ}$  and  $V_{DSQ}$ .
4. Use the measured  $I_{DSS}$ ,  $V_P$  and measured resistance values to perform PSPICE simulation. Summarize your simulation results. Compare  $I_{DQ}$  and  $V_{DSQ}$  obtained from the simulation with the ones obtained from step 1 and step 3.