

## JFET Amplifier Design

You are to design an amplifier using an n-channel JFET. **For uniformity, we will assume that the pinchoff voltage is  $-5\text{ V}$ , and the  $I_{DSS}$  is  $10\text{ mA}$ .** NOTE THAT ALL RESISTORS AND CAPACITORS ARE ASSUMED TO HAVE THEIR MARKED VALUES. Use **5% tolerance resistors, and 10% tolerance capacitors (Table C.4).** Assume  $V_{DS} \approx 10\text{ V}$ .

	JFET	Unit
Supply Voltage	20	V
Gain (magnitude)	$2.5 \pm 0.1$	V/V
Input resistance	3 MEG	$\Omega$
Output resistance	5 k	$\Omega$
Estimated lower – 3 dB cutoff frequency	$10 < f_L < 100$	Hz

The input impedance is a minimum permissible value.  
The output impedance is a maximum permissible value.

Your submissions are to be (in order)

1. A full page schematic of your FINAL design with all parts values indicated
2. A narrative first-pass design procedure for all parts values, with the design value of each enclosed in a box. Make sure that the JFET is biased in the saturation region.
3. A spreadsheet that calculates the values of each of the parameters that is specified. The first row in the spreadsheet MUST be the values calculated in your first-pass design procedure. It is expected that the last line on your spreadsheet will contain the values of resistance that are given on the front page. If this is not the case, the line corresponding to that schematic must be highlighted in the spreadsheet. The spreadsheet is to be progressive. That is, each line is to be a modification of the design on the previous line that aims to improve one or more specs of the previous design.
4. Perform PSpice simulation to plot the magnitude response and indicate its lower -3 dB cutoff frequency. Explain your simulation results.
5. Perform PSpice simulation to determine the maximum up/down voltage swings at the output. Explain your simulation results.