

Hede Ma

(U.S. Citizen)

Dept. of Electrical and Computer Engineering
California State University
Chico, CA 95929-0888
Phone: (530) 898-4957 (Office)
Fax: (530) 898-4956
E-mail: hma@csuchico.edu

18 Laguna Point Rd.
Chico, CA 95928
Phone: (530) 898-9488

Education

Ph.D. in Electrical Engineering, Degree Conferral Date: 5/18/1990
State University of New York at Binghamton
Binghamton, NY 13901, U.S.A.
Doctoral Dissertation Title: Efficient Fault Isolation Schemes for Grey Digital Systems

M.S. in Computer Engineering, Degree Conferral Date: 12/28/1982
Shanghai University of Science and Technology
Shanghai, China
Theses Title: Modeling and Analyzing Packet Switching Networks by Petri Nets

B.S. in Electrical Engineering, Degree Conferral Date: 7/26/80
Shanghai University of Science and Technology
Shanghai, China
Graduation Design Project: Programmable Logic Controller for 125 Ton Press Forging Machine

Professional Employment

Research Fellow, Summer 2004 - 2003
NASA Jet Propulsion Laboratory
Reliability Engineering, Section 513
Mail Stop 122-107
4800 Oak Grove Drive
Pasadena, CA 91109-8099

Professor, 2000 – present
Department of Electrical and Computer Engineering
California State University
Chico, CA 95929-0888

- Teaching Graduate and Undergraduate courses: **ECE 345 High-frequency Design Techniques**, **ECE 357 Electromagnetic Compatibility**, **ECE 397 VLSI Design**, **ECE 388 Computer-Aided Circuit Engineering**, **ECE 185 Logic Design**, **ECE 188 Computer Interface Circuits**, **ECE 140 Linear Circuits**, **ECE 145 Electronics**, etc. using such CAD and CAE software as Altera MAX+PLUS II 10.0, Xilinx UA-ISE-FND, Cadence SPICE, LogicWorks, Logic Aid, Cadence Layout Plus, and programming languages C++, VHDL, as well as FPGAs: Altera EPM7160, EPF10K, FLEX10K, UP 1, etc.
- Advisor of the project team winning the first place of IEEE EMC Society's 2001 Best Student Design, which was an international competition on EMI mitigation techniques in circuit designs.
- Counselor, IEEE CSU, Chico
- Advisor of Association of Computer Engineers.
- Doing research in areas of Error Detection and Fault Isolation, Design for Testability, Design for Reliability, Fault-Tolerance, VHDL, FPGA, and EMC.

Associate Professor, 1995 - 2000

Chairman of Electrical Engineering Laboratory Committee, 1996 - 1999
Department of Electrical and Software Engineering
University of Wisconsin
Platteville, WI 53818

Software Engineer, 1998 – 2000 (Summer full-time, School year part-time)

Avista, Inc.
Platteville, WI 53818
- Did hardware and software testing for the projects of Rockwell Collins **GLU/GNLU ILS** (Global Landing Unit/Global Navigation Landing Unit Instrument Landing System), **Boeing 767**, Sundstrand **Airbus390**.

Computer Engineer, 1997 (Summer Job)

NewTek, Inc.
8200 IH 10 West #900
San Antonio, TX 78230

Assistant Professor, 1990-1995

Acting Chairman, 1994

Director of Engineering Research Laboratories, 1993-1995
Dept. of Engineering
Savannah State University
Savannah, GA 31404

Research/Teaching Assistant (Ph. D. Student), 1985-1990

Dept. of Electrical Engineering
State University of New York (SUNY) at Binghamton
Binghamton, NY 13901

Visiting Scholar, 1984-85

Thomas J. Watson School of Engineering
State University of New York at Binghamton
Binghamton, NY 13901

Lecturer, 1983-1984

College of Computer
Shanghai University of Science and Technology
Shanghai, China

Publications

1. H. Ma, "CMOS Integrated Circuit Designs with LASI," In Proc. 2002 COC National Conference, Myrtle Beach, South Carolina, Nov. 10 – 13, 2002.
2. H. Ma, "Automatic Fault Isolation for reliable Design of Digital Systems," In Proc. 12th International Conference on Electronics, Communications and Computers, IEEE, Acapulco, Mexico, Feb. 25 – 28, 2002, pp.116-120.
3. H. Ma, "Gery Digital System Testing," In Proc. 12th International Conference on Electronics, Communications and Computers, IEEE, Acapulco, Mexico, Feb. 25 – 28, 2002, pp.105-110.
4. H. Ma, "PCB Design with EMI Mitigation Techniques Using OrCad 9.2 and National Semiconductor's Web Bench," In Proc. 2001 COC National Conference, Myrtle Beach, South Carolina, Nov. 11 – 14, 2001.
5. H. Ma, "Design for Testable Four-Channel Data Transfer Controller Using VHDL," In Proc. 11th

- International Conference on Electronics, Communications and Computers, IEEE, University of Americas-Puebla, Cholula, Puebla, Mexico, Feb. 22 – 24, 2001, pp.129-132.
6. H. Ma, "Software Test: Theory and Practice," In Proc. 11th International Conference on Electronics, Communications and Computers, IEEE, University of Americas- Puebla, Cholula, Puebla, Mexico, Feb. 22 – 24, 2001, pp.141-143.
 7. H. Ma, "Digital system design using cutting-edge design automation software and field-programmable gate array chips," In Proc. 2000 COC National Conference, Myrtle Beach, South Carolina, Nov. 12 – 15, 2000, pp.58-62.
 8. H. Ma, "Development of a new software Engineering program and curriculum," The 60th ASEE Midwest Conference, Winona, MN, Oct. 8-10, 1998.
 9. H. Ma, "Applications of Design Automation Software for Rapid Prototyping of Digital Systems," The 60th ASEE Midwest Conference, Winona, MN, Oct. 8-10, 1998.
 10. H. Ma, "Bus Expansion Card Design in Microcomputer Architecture and Interfacing," In Proc. The 59th ASEE Midwest Conference, Iowa City, IA, Oct. 9-11, 1997, pp.111-116.
 11. H. Ma, "Engineering Consulting and Engineering Education," In Proc. The 59th ASEE Midwest Conference, Iowa City, IA, Oct. 9-11, 1997, pp.41-45.
 12. H. Ma, "Functions of Final Projects and Project Teams in Computer Engineering Education," In Proc. The 59th ASEE Midwest Conference, Iowa City, IA, Oct. 9-11, 1997, pp.21-26.
 13. H. Ma, "The Necessity of A New Engineering Course - Patent It Yourself," In Proc. The ASEE/PSW 1997 Conference, San Luis Obispo, CA, Mar. 14-15, 1997, pp.129-133.
 14. H. Ma, "Altera FPGA Applications and Advanced Digital Design," In Proc. The 58th ASEE Midwest Conference, Fargo, ND, Sep. 3-5, 1996, pp.31-37.
 15. H. Ma, "Engineering Laboratories and Engineering Education," In Proc. The 58th ASEE Midwest Conference, Fargo, ND, Sep. 3-5, 1996, pp.51-55.
 16. H. Ma, "Pattern recognition using Boltzmann machine," In Proc. IEEE Southeastcon'95, Raleigh, NC, March 26-29, 1995, pp.23-29.
 17. H. Ma, "A customer-oriented test - estimation test," In Proc. 1994 IEEE Southeastcon'94, Miami, FL., April 11-13, 1994, pp.241-245.
 18. H. Ma, "A new testing philosophy - differential test," In Proc. 1993 IEEE Southeastcon'93, Charlotte, NC., April 5-7, 1993, pp.6-9.
 19. Y. Liu and H. Ma, "Macrocode for error detection and correction in mass memories," In Proc. 1993 IEEE Southeastcon'93, Charlotte, NC., April 5-7, 1993, pp.201-207.
 20. Y. Liu and H. Ma, "A simulation of macrocode for error detection and correction in mass memories," In Proc. 1993 International Simulation Technology Conference , Clear Lake, Texas, Nov. 4-6, 1992, pp.139-144.
 21. H. Ma, "An efficient simulator for automatic isolation of intermittent faults in digital systems," In Proc. The 40th Computer Simulation Conference, Reno, Nevada, July 27-30, 1992, pp.250-254.
 22. Y. Liu and H. D. Ma, "Image analysis using class 2 and class 5A dynamical systems," In Proc. The 45th Conference of The Society for Imaging Science and Technology, East Rutherford, NJ., May 10-15, 1992, pp.201- 204.
 23. Y. Liu and H. Ma, "Image analysis using class 3 and class 5B dynamical systems," In Proc. The 45th Conference of The Society for Imaging Science and Technology, East Rutherford, NJ., May 10-15, 1992, pp.205- 208.
 24. H. Ma and Y. Liu, "Automatic fault isolation techniques for digital systems," In Proc. IEEE Southeastcon'92, Birmingham, AL, April 12-15, 1992, pp.335-338.
 25. H. Ma and Y. Liu, "A testable design to test pattern sensitive faults efficiently for semiconductor random access memories," In Proc. IEEE Southeastcon'92, Birmingham, AL, April 12-15, 1992, pp.339-342.
 26. Y. Liu and H. Ma, "A comparison of two learning philosophies," In Proc. IEEE Southeastcon'92, Birmingham, AL, April 12-15, 1992, pp.247-254.
 27. Y. Liu and H. Ma, "Comparison between image analysis using class 2 and class 3 dynamical systems," Image Processing Algorithms and techniques III, James R. Sullivan, Editors, Proc. SPIE 1657, 1992, pp.461-475.

28. H. Ma and Y. Liu, Pattern recognition using ω -orbit finite automata," In Proc. Visual Communications and Image Processing'91: Image processing, Boston, MA, Nov. 11-13, 1991, pp.226-240.
29. H. Ma and Y. Liu, "Algorithms for moving object pattern recognition using ω -orbit finite automata," In Proc. 1991 International Simulation Technology Conference, Orlando, FL, Oct. 21-23, 1991, pp.552-558.
30. Y. Liu and H. Ma, " Pattern recognition using the third and the fifth classes of dynamical systems," In Proc. The Sixth International Symposium on Methodologies for Intelligent Systems, (Poster Session), Charlotte, NC, Oct. 16-19, 1991, pp.83-94.
31. Y. Liu and H. Ma, " A parallel pattern recognition approach," In Proc. The 4th International Conference on Parallel and Distributed Computing Systems, Washington D.C., Oct. 8-11, 1991, pp.255-260.
32. H. Ma and Y. Liu, " Efficient placement of error checkers in VLSI systems," In Proc. Test Engineering Conference, Atlanta, GA, June 25-27, 1991, pp.103-111.
33. H. Ma and Y. Liu, "Self-verification of semiconductor random access memories," In Proc. Test Engineering Conference, Atlanta, GA, June 25-27, 1991, pp.113-118.
34. Y. Liu and H. Ma, " ω -orbit finite automata and image compression," In Proc. 44th Annual Conference of the Society for Imaging Science and Technology, St. Paul, Minnesota, May 12-17, 1991, pp.489-492.
35. H. Ma and Y. Liu, " Functional testing of digital systems described by AHDL," In Proc. 22nd Annual Conference on Modeling and Simulation, Pittsburgh, PA, May 2-3, 1991, pp.1644-1651.
36. H. Ma and Y. Liu, "Design for diagnosable multipleoutput digital systems," In proc. IEEE VLSI Test Conference, Atlantic City, NJ, April 15-17, 1991, IEEE Computer Press, pp.204-209.
37. Y. Liu and H. Ma, " ω -orbit finite automata for data compression," In Proc. IEEE Data Compression Conference, Snowbird, Utah, April 8-11, 1991, IEEE Computer Press, pp.166-175.
38. H. Ma and Y. Liu, "Necessary and sufficient conditions for efficient fault isolation in digital systems," In Proc. 25th Annual Conference on Information Sciences and Systems (CISS) 1991, The Johns Hopkins University, Baltimore, MD, March 20-22, 1991, pp.868-873.
39. H. Ma, Efficient Fault Isolation Schemes for Grey Digital Systems, Ph.D. dissertation, State University of New York, Binghamton, NY, May, 1990.
40. S. Y. H. Su and H. Ma, "Design for Diagnosability and reliability in VLSI systems," In Proc. IEEE International Test Conference, Washington D. C., 1988, pp.888-897.
41. S. Y. H. Su and H. Ma, "Fault isolation in grey digital systems," In Proc. IEEE International Test Conference, Washington D. C., 1988, pp.54-63.
42. H. Ma and T. N. Rajshakahara, "A testable design of semiconductor random access memories," In Proc. 30th Midwest Conference on Circuits and Systems, Syracuse, NY, 1987, pp.540-543.
43. H. Ma, "Livelock avoidance in packet switching networks," In Proc. The Computer Conference of Shanghai, Shanghai, China, 1983.
44. H. Ma, Modeling and Analyzing Packet Switching Network by Petri Nets, M.S. thesis, Shanghai University of Sciences and Technology, Shanghai, China, December, 1982.

Presentations

1. H. Ma, "Reliability Design Methodologies and Tool Evaluation Plan," NASA Jet Propulsion Laboratory, Pasadena, CA 91109-8099, June. 8, 2003.
2. H. Ma, "Mitigation Techniques for Electromagnetic Compatibility," NASA Jet Propulsion Laboratory, Pasadena, CA 91109-8099, Aug. 6, 2003.
3. H. Ma, "Grounding Techniques," NASA Jet Propulsion Laboratory, Pasadena, CA 91109-8099, Jul. 18, 2003.
4. H. Ma, "Decoupling Techniques," NASA Jet Propulsion Laboratory, Pasadena, CA 91109-8099, Jul. 25, 2003.
5. H. Ma, "Crosstalk," NASA Jet Propulsion Laboratory, Pasadena, CA 91109-8099, Aug. 1, 2003.
6. H. Ma, "Hardware/software Codesign and Rapid Prototyping of Embedded Systems," LCI Semiconductor Research Institute, Shanghai, China, June 18, 2001.
7. H. Ma, "Digital System Design with VHDL," Shanghai University, Shanghai, China, June 8, 2000.
8. H. Ma, "Software Test: Theory and Practice," Chaoyang University, Taiwan, Oct. 22, 1998.

9. H. Ma, "Rapid prototyping of Digital Systems," Institute of China East Computing Techniques, Shanghai, China, Jan. 7, 1998.
10. H. Ma, "Implementation of Artificial Intelligence with Integrated Circuit Designs," IEEE Savannah Section, Savannah, Georgia, May, 1994.

Grants

1. Altera hardware donation, IP-EMAC MegaCore, \$12,995, NIOS Stratix Pro Development Kit, \$2,495, MAX+PLUS II Fixed Node Subscription, \$2,000, for a total equipment grant of **\$17,490**, from Altera, Inc., 2004.
2. Summer Scholarship, **\$4,000**, California State University, 2003.
3. Xilinx hardware equipment grant (UW-V1000-DK) **\$244,305** from Xilinx, Inc., 2002.
4. Altera supplementary donation, MAX+PLUS II Fixed Node Subscriptions of 20 for PC, including updates, valued at \$2,000 each per year, for a total equipment grant of **\$40,000**, from Altera, Inc., 2002.
5. Magic XII, Magic 4.0, and DOS Magic for VLSI integrated circuit design and layout, donated by the Software Distribution Office, University of California, Berkeley, 2002.
6. Center for excellence in learning and teaching, **\$300**, from California State University, Chico, 2002.
7. Cadence Pspice A/D (\$4,495 each), Capture (\$1,495 each), and Layout Plus (\$11,495 each), fourteen seats valued at \$17,485 each, one Optimizer priced at \$3,995, plus the lifetime updates for the fourteen seats (\$1,440 per seat for the year of 2001, where Layout Plus \$768 per seat, Capture \$108 per seat, Pspice A/D \$564 per seat), totaling **\$268,945**, from Cadence, Inc., 2001.
8. Xilinx UA_ISE_FND (\$2,495 each), thirty-four seats valued at \$84,830, one US-ISE-FND priced at \$2,495, and six DIGILAB-XL-A5 valued at \$744, totaling **\$88,069** from Xilinx, Inc., 2001.
9. Altera Design Lab Package (UP 1 Board), five UP 1 boards valued at \$695, one PLMJ7000-84 Programming Adapter valued at \$375, 50 EPM7032LC44-10 devices valued at \$9.80 each, fifteen seats of MAX+PLUS II Fixed Node Subscriptions for PC, including updates, valued at \$2,000 each per year, for a total equipment grant of **\$34,340**, from Altera, Inc., 2001.
10. Summer Scholarship, **\$4,000**, California State University, 2001.
11. Robot Design Project for Association of Computer Engineers, CSU, Chico, **\$500**, from Dr. Bill Wattenburg, 2001.
12. Integrated Circuit Designs for Artificial Intelligence and Neural Networks, Scholarly Activity Improvement Fund, **\$3,998**, from University of Wisconsin, 1999.
13. Software Engineering improvement, Professional Development Fund, **\$700**, from University of Wisconsin, 1999.
14. A First Step Towards A Software Engineering Program at University of Wisconsin – Platteville, Curriculum Improvement Fund, **\$3,000**, from University of Wisconsin, 1998.
15. Max+Plus II 9.1, **\$126,000**, from Altera, Inc., 1997.
16. Pattern recognition using Boltzmann machine, **\$7,000**, from Oak Ridge National Laboratories Oak Ridge, 1994.
17. Laboratory Equipment Grant, **\$239,000**, from University System of Georgia, 1994.

Courses Taught

I have taught the following Graduate and Undergraduate courses in California State University and University of Wisconsin.

1. ECE 357 Electromagnetic Compatibility (New graduate course created by Hede Ma)
2. ECE 397 VLSI Design (New graduate course created by Hede Ma)
3. ECE 388 Computer-Aided Circuit Engineering (New graduate course created by Hede Ma)
4. ECE 345 High-frequency Design Techniques
5. ECE 188 Computer Interface Circuits
6. ECE 145 Electronics I
7. ECE 140 Linear Circuits

8. ECE 195 Computer Simulation Laboratory
9. ECE 085 Logic Design Fundamentals
10. ECE 030 Electricity and Instruments
11. EE 472 Microcomputer Architecture and Interfacing
12. EE 372 Introduction To Microprocessors
13. EE 475 Advanced Digital Systems
14. EE 371 Logic and Digital Design
15. EE 221 Circuit Modeling II
16. EE 121 Circuit Modeling I
17. CE 233 VLSI Design
18. CE 203 Principles of Computer Electronics
19. EE 323 Microcomputer Systems
20. EE 431 Transmission Line and Microwaves
21. EE 313 Solid State Electronic Devices
22. EE 302 Electronic Circuits
23. EE 301 Electronic Principle II
24. EE 203 Electronic Principle I
25. EE 201 AC Circuit Analysis I
26. EE 103 DC Circuit Analysis

Affiliations and Awards

IEEE Counselor, CSU, Chico, 2003-present
 Member, IEEE, 1987-present
 Member, ACM, 1992-present
 Member, Sigma Xi Scientific Research Society, 1992 – present
 Secretary/Treasurer, Sigma Xi Scientific Research Society Savannah Chapter, 1993-94
 Member, ASEE, 1996 – present
 Member, IEEE Technical Committee on test engineering, 1990-present
 Member, IEEE Technical Committee on Software Engineering, 1993-present
 Chairman, IEEE Student Activities Committee, IEEE Savannah Section, 1992-95
 Counselor, IEEE Student Chapter, Savannah State University, 1991-95
 Outstanding Faculty, Dept. of Engineering, Savannah State University, 1994
 Referee, IEEE Proceedings on Computers and Digital Techniques, 1997 - present
 Referee, IEEE Transaction on Computer, 1990
 Judge, Science and Engineering Fair, Savannah, Georgia, 1991-1994
 Chairman, Student Association of China, State university of New York at Binghamton, 1986-87
 Senator, Graduate Student Organization, State University of New York at Binghamton, 1985-86
 Graduate Scholarship, SUNY at Binghamton, New York, 1985-90
 Senior Scholarship, Ministry of Education of China, 1984-85
 Graduate Scholarship, Shanghai University of Sciences and technology, Shanghai, China, 1980-82